ECE 522: Two-Stage Single Ended CMOS Op-Amp

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***Abstract*—This project report will present a two stage op-amp design to fulfill the project requirements for CMOS Integrated Circuits Course— ECE522 at Oregon State University (OSU). A comparison of simulated results and specifications is listed in the report. The simulated results will be presented in the report, along with a discussion on some of the subtle design techniques employed from the ECE422/522 class at OSU. Supporting documentation for the design analysis will be attached in the appendix of this report.**

***Index Terms*— Amplifiers, CMOSFET Amplifiers, FET Amplifiers, Operational Amplifiers.**

I. Introduction

THIS report purports one of many possible design techniques for the two-stage op-amp which is presented in the CMOS Integrated Circuits Course ECE522 at Oregon State University (OSU). The two-stage op-amp topology follows the classical differential input, single-ended output framework, with included Miller compensation capacitor and zero-nulling resistor. The project parameters will be compared via tables to the actual specifications achieved. A schematic will presented which shows the final design reached. Some of the design subtleties will be discussed as well throughout the paper.

II. Design Approach

The project specifications require the Bsim3 MOSFET model to be used for project simulation of both PMOS and NMOS transistors. To start the project, the path was followed of extracting Level 1 MOSFET model parameter equivalents from the Bsim3 model. The gate and drain of a single Bsim3 MOSFET were connected to dc voltage supplies, and the supplies were swept for current vs. V_{gs} parameterization characteristics of the BSIM3 model. The basic k, V_T, γ, λ, and V_{TO} parameter extraction methods were then reviewed in the ECE522 course notes. An initial design step was taken of finding the V_{GS}-I_D curves for the BSIM3 model as can be seen in Figure 1. Then, the design process deviated to the circuit from homework #6, which is almost identical. It was used as a jumping off point for doing analysis, when paired with the homework #8 guide on adjusting parameters in the two-stage op-amp.

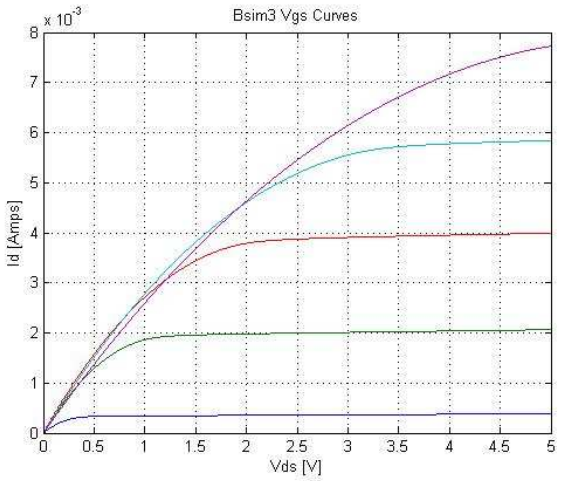

Fig. 1. NMOSFET V_{DS} vs. I_{DS} curves extracted from the Bsim3 model using HSPICE. The various traces ascend upward in terms of their V_{GS} values which ranged between one and five volts. This traditional path of design was eventually abandoned for a more rapid design approach. Refer to Appendix 1-2 for HSPICE & MATLAB code.

The design approach started with the ECE522-homework #6 two-stage design, which was updated to include the correct load capacitor value, zero-nulling resistor addition, and parameterization of the widths and lengths of the MOSFETS. The Level 1 MOSFET model was also changed to the BSIM3 model at this point. The area equations for the transistor drain/source perimeter and area calculations were imbedded into the SPICE netlist for automatic calculation so that simpler changes could be made to the basic parameters from the top of the SPICE file.

The next step in the design process was to make sure all MOSFETs were in saturation. The circuit did not require any adjustment in this initial step because it satisfied the requirements for saturation.

With saturation requirements satisfied, the next step in the process was to use the design parameter table derived homework #8 to adjust the various project parameters for meeting project specification. Since there were multiple parameters to meet, the open-loop gain was chosen as a starting point. To increase the open-loop gain, a few steps were taken. One step was to decrease the width of current reference mirroring MOSFET, M_8, so that it would cause a larger mirror of currents to the stage one and two current sources, M_7 and M_6. Also, the differential input positive and negative transistors had their widths increased. This benefited in a larger g_m for the first stage of signal amplification. A

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focus was made on increasing the g_m of stage one because it had the smaller transconductance of the two gain stages. This was done primarily to the first stage of the op-amp because it had a lower g_m.

The first stage gain increase caused the op-amp to meet gain requirements for the project, but frequency requirements were not met because of a phase margin (PM) less than 60°. To increase the phase margin, the nulling resistor which was added to cancel the second pole of the circuit and also to shift the second pole frequency higher in the frequency domain. This was able to give the amplifier a higher unity gain bandwidth, and a high enough phase margin to easily exceed specifications. Although the nulling resistor value was calculated via the inverse of the transconductance of M_3, it was found that a larger value did a better job of pole splitting.

After the first successful design cycle (which did include multiple revisions) was completed, the results were saved. Then a new design cycle was started in an attempt to get the open loop gain higher for the circuit, the phase margin larger for the circuit, and the unity gain frequency higher for the circuit. Each of the design revisions undertook a similar process which employed the design parameter table from homework #8. After the fourth design revision, the final values for the amplifier were chosen and kept at the values seen in the schematic of Figure 2, and listed in Table 1.

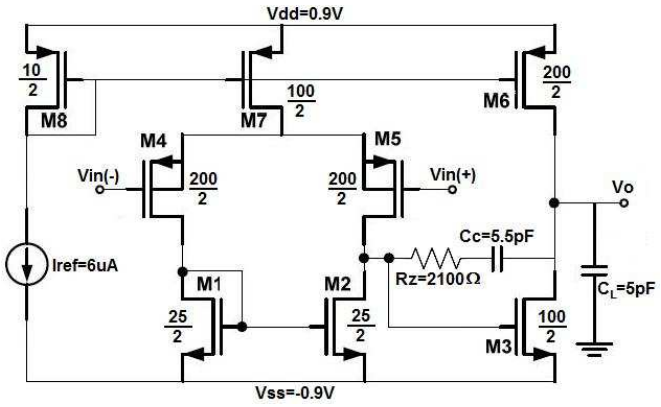

Fig 2. Schematic of the Two-Stage Op-Amp project. Supply voltages and currents are listed along with the width & length of each MOSFET. Note the (+) and (-) inputs.

The couple capacitor was adjusted to twice its current value during simulation to see what results it would have. It was found as to be expected that the unity-gain frequency went down when the coupling capacitor value was doubled. When the coupling capacitor value was decreased to one fifth its current value, it was also found that the unit gain frequency went down, which is assumed to be due to a lack of pole splitting.

Design Constraints and Parameters			
Variable	**Constraint**	**Specification**	**Units**
Vdd	+0.9	+0.9	V
Vss	-0.9	-0.9	V
W1-2	≥ 0.18	25	µM
W3, W7	≥ 0.18	100	µM
W4-6	≥ 0.18	200	µM
W8	≥ 0.18	10	µM
L1-8	≥ 0.18	2	µM
Cc		5.5	pF
CL	5	5	pF
R		2100	Ω
Iref		6	µA

Table 1. Final physical specifications and sizing of parts compared to original project design constraints.

Each design cycle revision required a check of the saturation state of all MOSFETs from the operating point analysis of HSPICE. These saturation states can be seen in Appendix #9 under MOSFET Operating Point Analysis. The open loop gain was also checked each time by means of a transfer function calculation that HSPICE performed on the netlist. Pole-Zero analysis was used to determine how well the nulling resistor was causing frequency alignment between the right-half-plane zero and the second pole. Finally, MATLAB was used to look at the bode plot results of an AC swept input for verifying whether the phase margin and unity gain frequency requirements were met.

III. Results

The results of the HSPICE analysis can be seen in Table 2. The open loop gain of the circuit is approximately 15 dB above the requirement. The unity-gain frequency is approximately 5 MHz above the project specified system frequency, which gives a desirable wider system bandwidth. The phase margin is also 12.5° higher than required which will make the circuit more stable. The open loop gain, unity gain frequency, and phase margin were all calculated using ac-analysis in MATLAB which was originally generated in HSPICE. The power calculation was performed by hand. The current through each "leg" of the main current source was multiplied by the rail-to-rail voltage. These three separate powers were then summed for the total system power under no additional load. $V_{IC\text{-}MAX}$ and $V_{IC\text{-}MIN}$ were determined through hand calculation, and then confirmed through HSPICE dc sweep analysis. The input referred noise (IRN) was calculated using HSPICE analysis. To determine the power supply rejection ratio (PSRR), a combination of HSPICE analysis and hand calculations were used.

Specifications and Performance			
Variable	**Constraint**	**Specification**	**Units**
Open Loop Gain	> 65	80.76	dB

Unity Gain Frequency	> 12	17.14	MHz
Phase Margin	> 60	72.5	° (angle)
Power (5pF load)	-	339.8	µW
Vic-min		-0.76647	V
Vic-max		0.18878	V
I. R. N. at 1kHz		-261	dB
I. R.N. at 10MHz		-317	dB
P.S.R.R. -Vdd at 1kHz		98.92	dB
P.S.R.R. -Vdd at 10MHz		32.294	dB
P.S.R.R. -Vss at 1kHz		80.114	dB
P.S.R.R. -Vss at 10Mhz		3.598	dB

Table 2. Final Performance Specifications with project constraints and final project specifications listed side-by-side for comparison.

The performance values in Table 2 correlate with the following Figures 1 through 7 and Equations 1 through 7 as follows below.

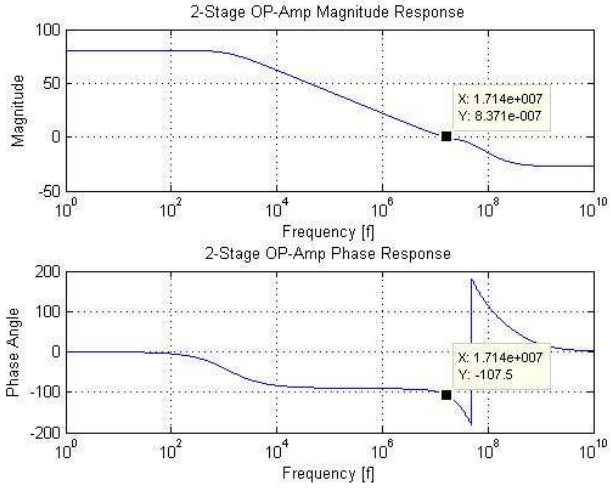

Fig 3. Bode plot of system magnitude in decibles and phase angle offset from input to output based on frequency. Unity-gain frequency listed in box of Magnitude plot. Unity-gain frequency point marked in phase angle plot.

These are the plots which describe the fundamental quantities in the circuit, specificly the Unity Gain Bandwidth, the Open Loop Gain, and the Phase Margin. Their measured results are shown in Table 2. Appendix 3 HSPICE and MATLAB show the code used to generate these plots.

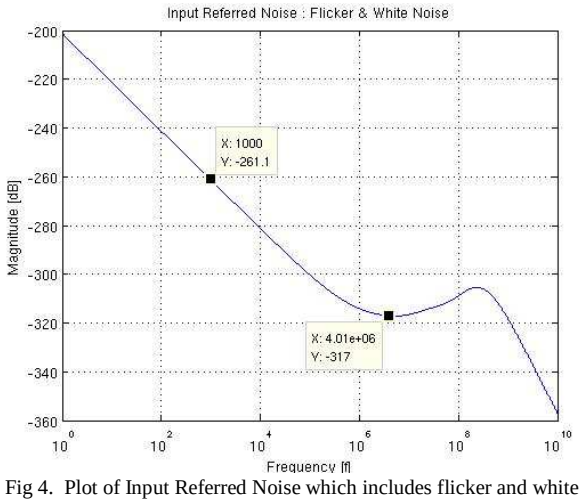

Fig 4. Plot of Input Referred Noise which includes flicker and white noise. The 1KHz and 4MHz magnitudes are marked on the graph.

The input referred noise shown in Figure 4 was generated with the given noise parameters which were added to the BSIM3 model by hand. These values were KF for an NMOS = 1E-26 and KF for a PMOS = 1E-27. Figure 4 shows that the noise decreases with an increase in frequency.

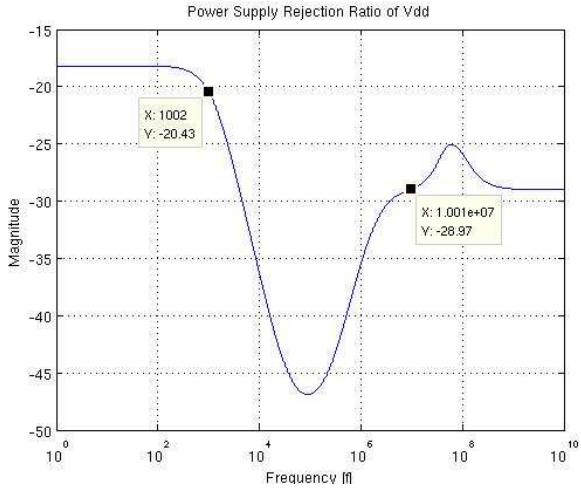

Fig 5. Plot of Power Supply Rejection from V_{DD} to V_{OUT}. The frequencies 1KHz and 10MHz are marked on the graph.

The power supply rejection ratio (PSRR) was calculated using Equations listed in 7. The PSRR is equal to the gain of the output vs. the gain of the power supply at a given frequency. The simulated values are given in Table 2 for both the negative and positive supply. PSRR is performed with an AC sweep from the input to the output of a circuit, with the AC source connected to a specific supply rail. Because there are two supply rails, there are two PSRR numbers for this particular circuit.

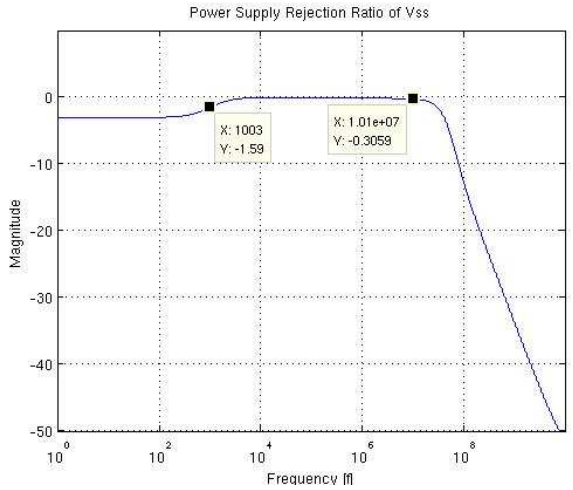

Fig 6. Plot of Power Supply Rejection from V_{SS} to V_{OUT}. The frequencies 1KHz and 10MHz are marked on the graph.

The magnitude dB values in the Figure 6 PSRR plot were used to calculate the respective PSRR values in Table 2. The equations used to calculate PSRR are seen in Equation set 3.

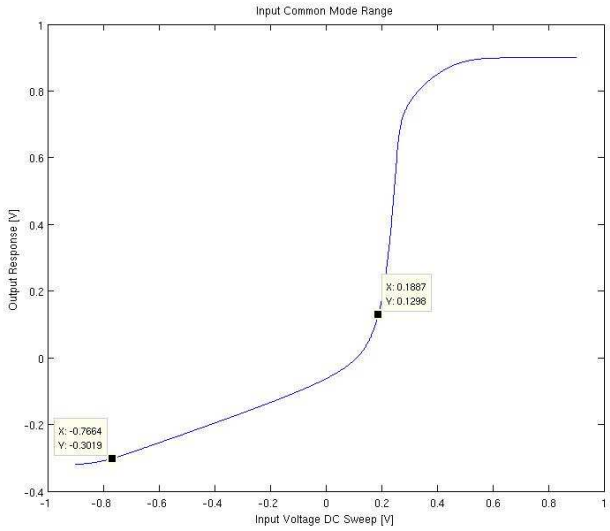

Fig 7. Plot of input common mode range. $V_{IC\text{-}MIN}$=-0.76647 V, $V_{IC\text{-}MAX}$=0.18878 V

One observable difference between hand calculations and the graphical result of MATLAB can be seen in Figure 7 which is the plot of input common mode range vs. output response. Equation 1 shows the V_{IC} equations which were used to calculate the minimum and maximum. It could be that during the higher gain range of Figure 7, some MOSFETs are going into triode or cutoff.

IV. Applicable Equations / Equations Used

$$V_{IC-MIN} = V_{SS} + |V_{GS1}| - V_{TP}$$
$$V_{IC-MAX} = V_{DD} + |V_{TP}| - |V_{GS7}| - |V_{GS4}|. \quad (1)$$

$$g_m = \sqrt{2 I_D k' \frac{W}{L}} \quad (2)$$

.

$$PSRR^+ = \frac{A_{dm}}{A^+}$$
$$PSRR^- = \frac{A_{dm}}{A^-} \quad (3)$$

.

$$\omega_C = \frac{G_{M1}}{C_C} \quad (5)$$

.

$$Rz = \frac{1}{G_{M2}} \quad (6)$$

.

$$K_N = \frac{2 \times (slope)^2}{\frac{W}{L}} = 143 \frac{uA}{V^2}$$
$$K_P = \frac{2 \times (slope)^2}{\frac{W}{L}} = 32 \frac{uA}{V^2} \quad (7)$$

.

V. Conclusion

A two-stage op-amp design was presented, the design process undertaken was discussed, and the resulting simulation and analysis was presented. For ECE522, this was a good starter design project, but as the results show, there are many areas of consideration which were not specified for this project. For instance specified common-mode range, output swing, slew rate, and power requirements are a few of the possible requirements which may be imposed in future design projects. The stronger a design engineer is with the fundamental basic analog building blocks, the better a job they will do at designing analog circuits such as this two-stage op-amp. It is not to be thought of as a solution to a need for op-amps, but rather a stepping stone which connects people to a vast array of op-amp possibilities and configurations, with the two-stage op-amp presented being one of the starter building blocks.

Appendix

Appendix 1) HSPICE for NMOSFET V_{DS} vs. I_{DS} curves

```
**************************************************
*   ECE-522 ~ NMOSFET VDS vs. IDS curves
*   Christopher Haller
*   Simulation for VDS vs. IDS curves W.R.T. VGS
*   Based on code from class GTAs Jon & Mohsen
**************************************************
.options post node
.options runlvl=0
.include "Bsim3_p18.lib"
.temp   25
$$$$$$$$$  Independent Sources   $$$$$$$$$$$$$$$$$$
  Vds     vds     gnd     DC      5
```

```
  Vgs     vgs     gnd     DC      2
  Vss     vss     gnd     DC      0
  Vbs     vbs     gnd     DC      0
$$$$$$$$$   Transistors   $$$$$$$$$$$$$$$$$$$$$$$$
  X_M1  vds  vgs  vss  vbs  CMOSN  +W=10u  +L=1u  ad=20p
as=20p pd=24u ps=24u
  $$$$$$$$$   Analysis   $$$$$$$$$$$$$$$$$$$$$$$$
  .op     $Operating Point Analysis
  .dc vds 0 5 .001 vgs 1 5 1
  .plot -i(vds)
  .end
```

Appendix 2) MATLAB Code for NMOSFET V_{DS} vs. I_{DS} curves

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% CAH : BSIM3 Curve Trace Plot for Vgs vs. Id
% 2007 December 11
% ECE522 Final Project
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
clc;
clear;
addpath('z:\Classes\ECE522\project\Bsim3_curves\H
spiceToolbox\')
x=loadsig('curves.sw0');
lssig(x)
plotsig(x,'abs(I_vds)');
title('Bsim3 Vgs Curves');
xlabel('Vds [V]');
ylabel('Id [Amps]');
```

Appendix 3) HSPICE Code for "Project" – Master Netlist

```
  project.sp
  ************************************************
************
  *   ECE-522 ~ Nov 18, 2008 ~ Final Project
  *   Christopher Haller
  *   Simulations for 2-Stage Op-Amp final project
  *   Some small snippets of code based originally
  *   on code from class GTAs Jon & Mohsen
  *   2-Stage OP-AMP built on HW#6 Model
  ************************************************
************
  .options post node
  .options runlvl=0
  .include "Bsim3_p18.lib"
  $$$$$$   MOSFET Parameters   $$$$$$$$$$$$$$$$$$
  .param W_1 = 25u $ 1st stage (-)-side load
  .param W_2 = 25u $ 1st stage (+)-side load
  .param W_3 = 100u  $ 2nd stage amplifier
  .param W_4 = 200u  $ 1st stage negative input
  .param W_5 = 200u  $ 1st stage positive input
  .param W_6 = 200u  $ 2nd stage current source
  .param W_7 = 100u  $ 1st stage current source
  .param W_8 = 10u   $ current mirror
  .param L_all = 2u
  .param I_src = 6u
  $$$$$$$   Independent Sources   $$$$$$$$$$
  Vdd vdd gnd DC 0.9 $AC 1.0
  Vss vss gnd DC -0.9 $AC 1.0
  Icurrent Vx gnd I_src
  Vin_p vinp gnd DC 0
Vin_n vinn gnd DC 0  AC 1.0
  $$$$$$$$$$   Transistors   $$$$$$$$$$$$$$$$$$$$$$
  X_M1   Vz   Vz   vss   vss   CMOSN     W=W_1   L=L_all
AD='0.6u*W_1'      AS='0.6*W_1'      PD='1.2u+2*W_1'
PS='1.2u+2*W_1'
  X_M2   Vw   Vz   vss   vss   CMOSN     W=W_2   L=L_all
AD='0.6u*W_2'      AS='0.6*W_2'      PD='1.2u+2*W_2'
PS='1.2u+2*W_2'
  X_M3   Vo   Vw   vss   vss   CMOSN     W=W_3   L=L_all
AD='0.6u*W_3'      AS='0.6*W_3'      PD='1.2u+2*W_3'
PS='1.2u+2*W_3'
  X_M4   Vz   vinp   Vy   Vy   CMOSP     W=W_4   L=L_all
AD='0.6u*W_4'      AS='0.6*W_4'      PD='1.2u+2*W_4'
PS='1.2u+2*W_4'
  X_M5   Vw   vinn   Vy   Vy   CMOSP     W=W_5   L=L_all
AD='0.6u*W_5'      AS='0.6*W_5'      PD='1.2u+2*W_5'
PS='1.2u+2*W_5'
  X_M6   Vo   Vx   vdd   vdd   CMOSP     W=W_6   L=L_all
AD='0.6u*W_6'      AS='0.6*W_6'      PD='1.2u+2*W_6'
PS='1.2u+2*W_6'
  X_M7   Vy   Vx   vdd   vdd   CMOSP     W=W_7   L=L_all
AD='0.6u*W_7'      AS='0.6*W_7'      PD='1.2u+2*W_7'
PS='1.2u+2*W_7'
  X_M8   Vx   Vx   vdd   vdd   CMOSP     W=W_8   L=L_all
AD='0.6u*W_8'      AS='0.6*W_8'      PD='1.2u+2*W_8'
PS='1.2u+2*W_8'
  $$$$$$$   Passives   $$$$$$$$$$$$$$$$$$$$$$
  C1 Vo Vcap 5.5p
  C2 Vo gnd  5p   $Output Capacitor
  R1 Vw Vcap 2100 $%^800$%^2103  $.op
  $.noise v(vo) Vin_n
  .pz V(Vo) Vin_p
  .ac dec 10000 1 10g
  $.plot (vo)
  $.tf v(vo) Vin_p
  $.dc Vin_p -0.9 0.9 .001
  .end
```

APPENDIX 3) MATLAB Code for PHASE PLOT

```
  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
  % % %  CAH:  Magnitude and Phase Plot {bode}
  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
  % hspice command:    .ac dec 10000 1 10g
  % Use 1 V AC input ontop of 0 V DC input on Vin_in
  % Below MATLAB will graph results
  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
  clc;
  clear;
  addpath('Z:\Classes\ECE522\project\Bsim3_c
urves\HspiceToolbox\');
  x=loadsig('project.ac0');
  lssig(x) % The lssig command will list all of your
nodes in the Matlab main window
  plotsig(x,'db((vo)); (ph((vo)))','logx');
  subplot(2,1,1);
  title('2-Stage OP-Amp Magnitude Response');
  xlabel('Frequency [f]');
  ylabel('Magnitude');
  subplot(2,1,2);
  title('2-Stage OP-Amp Phase Response');
  xlabel('Frequency [f]');
  ylabel('Phase Angle');
  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

APPENDIX 4) MATLAB Code for Input Referred Noise Plot

```
  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
  %  CAH:  Input Referred Noise Plot
  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
  % hspice command:    .noise v(vo) Vin_n
  % hspice command:    .ac dec 10000 1 10g
  % Use 1 V AC input ontop of 0 V DC input on Vin_in
  % Below MATLAB will graph results
  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
  clc;
  clear;
  addpath('Z:\Classes\ECE522\project\Bsim3_curves\Hs
piceToolbox\');
  x=loadsig('project.ac0');
  lssig(x)
  plotsig(x,'db(innoise)','logx');
  title('Input Referred Noise : Flicker & White
Noise');
  xlabel('Frequency [f]');
  ylabel('Magnitude [dB]');
  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

APPENDIX 5) MATLAB Code for PHASE PLOT

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%  CAH:  PSRR^@ from Vdd and Vss
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% hspice command: .ac dec 10000 1 10g   {{{ONLY}}}
% Use 1VAC input ontop of 0 DC input on Vdd or Vss
% Each supply rail gets its own AC analysis.
% Below MATLAB will graph results
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
addpath('Z:\Classes\ECE522\project\Bsim3_curves\HspiceToolbox\');
clc;
clear;
x=loadsig('project.ac0');
lssig(x)
plotsig(x,'db((vo))','logx');
title('Power Supply Rejection Ratio of Vss');
xlabel('Frequency [f]');
ylabel('Magnitude');
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

APPENDIX 6) MATLAB Code for ICMR PLOT

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%  CAH:  ICMR Plot
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% hspice command:    .dc Vin_p -0.9 0.9 .001
% tie inputs together to same node 0Vdc and sweep
% Below MATLAB will graph results
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
addpath('/nfs/farm/u1/h/haller/Classes/ECE522/project/Bsim3_curves/HspiceToolbox/')
clc;
clear;
x=loadsig('project.sw0');
lssig(x)
a=evalsig(x,'vo');
b=evalsig(x,'vinp');
plot(b,a)
title('Input Common Mode Range');
xlabel('Input Voltage DC Sweep [V]');
ylabel('Output Response [V]');
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

APPENDIX 7) HSPICE Code for Pole / Zero Analysis

```
 project.sp
  ******   pole/zero analysis              tnom=  25.000 temp=  25.000
 ******

      input =  0:vin_p                output = v(vo


      input =  0:vin_p                output = v(vo

      poles (rad/sec)                 poles ( hertz)
**********************************************************************
    real            imag            real            imag
   -7.6320k         0.              -1.2147k         0.
  -11.9797x         0.              -1.9066x         0.
 -231.1756x       188.8054x        -36.7927x        30.0493x
 -231.1756x      -188.8054x        -36.7927x       -30.0493x
 -304.0473x       -99.3455x        -48.3906x       -15.8113x
 -304.0473x        99.3455x        -48.3906x        15.8113x
      zeros (rad/sec)                 zeros ( hertz)
**********************************************************************
    real            imag            real            imag
  -12.2415x        28.5456          -1.9483x         4.5432
 -120.8174x         0.              -19.2287x         0.
 -273.0681x         0.              -43.4601x         0.
  477.6073x         0.               76.0136x         0.
   -1.5008g        50.8527k        -238.8578x         8.0935k
    1.8779g         0.              298.8775x         0.

 ***** constant factor = -167.3835u      *****
```

APPENDIX 8) HSPICE Small Signal Transfer Characteristics

```
****     small-signal transfer characteristics
v(vo)/vin_p                    =  -10.9238k
input resistance at vin_p      =  1.000e+20
output resistance at v(vo)     =   63.0497k
```

APPENDIX 9) HSPICE Operating Point Analysis

Operating Point Analysis				
subckt	x_m1	x_m2	x_m3	x_m4
element	1:mn	2:mn	3:mn	4:mp
model	0:mosn	0:mosn	0:mosn	0:mosp
region	Saturati	Saturati	Saturati	Saturati
id	29.9643u	29.9643u	122.8716u	-29.9643u
ibs	0	0	0	0
ibd	0	0	0	0
vgs	553.1827m	553.1827m	553.1827m	-507.7181m
vds	553.1827m	553.1827m	836.4771m	-854.5354m
vbs	0	0	0	0
vth	398.8184m	398.8184m	397.2910m	-419.6517m
vdsat	120.4075m	120.4075m	121.4220m	-89.8650m
vod	154.3643m	154.3643m	155.8917m	-88.0664m
beta	3.5336m	3.5336m	14.1171m	7.5081m
gam eff	594.4536m	594.4536m	594.4625m	526.5899m
gm	389.7982u	389.7982u	1.5839m	475.5867u
gds	2.8471u	2.8471u	11.1134u	1.4847u
gmb	111.0454u	111.0454u	451.6784u	157.0652u
cdtot	39.4395f	39.4395f	153.2026f	250.3543f
cgtot	380.3975f	380.3975f	1.5219p	2.7649p
cstot	225.4312f	225.4312f	901.5228f	1.6385p
cbtot	157.5045f	157.5045f	624.7967f	1.1662p
cgs	339.1159f	339.1159f	1.3580p	2.4818p
cgd	17.4950f	17.4950f	69.5816f	115.1480f

Operating Point Analysis				
subckt	x_m5	x_m6	x_m7	x_m8
element	5:mp	6:mp	7:mp	8:mp
model	0:mosp	0:mosp	0:mosp	0:mosp
region	Saturati	Saturati	Saturati	Saturati
id	-29.9643u	-122.8716u	-59.9286u	-6.0000u
ibs	0	0	0	0
ibd	0	0	0	0
vgs	-507.7181m	-623.1538m	-623.1538m	-623.1538m
vds	-854.5354m	-963.5229m	-392.2819m	-623.1538m
vbs	0	0	0	0
vth	-419.6517m	-419.6517m	-419.6469m	-419.5612m
vdsat	-89.8650m	-165.3909m	-165.2687m	-163.5217m
vod	-88.0664m	-203.5021m	-203.5069m	-203.5926m
beta	7.5081m	7.2795m	3.6399m	364.2322u
gam eff	526.5899m	526.5899m	526.5824m	526.4472m
gm	475.5867u	1.1207m	548.4706u	54.8926u
gds	1.4847u	4.7471u	3.3353u	249.5921n
gmb	157.0652u	374.7244u	183.0086u	18.0414u
cdtot	250.3543f	247.1999f	136.9404f	13.0851f
cgtot	2.7649p	2.9163p	1.4619p	146.1007f
cstot	1.6385p	1.7555p	879.3540f	87.6285f
cbtot	1.1662p	1.1540p	588.7697f	58.5258f
cgs	2.4818p	2.6985p	1.3509p	134.6505f
cgd	115.1480f	115.2840f	60.5863f	5.8048f

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