Inter-Stage Gain Amplifier for a 13-bit 100Msamples/sec Two-Step ADC

Oregon State University

Christopher Haller **Divya Kesharwani**

haller@eecs.oregonstate.edu keshardi@eecs.oregonstate.edu

I. Design Approach

In order to develop the design of the opamp, the overall specifications necessary to meet the performance must commensurate with the choice of architecture and technology limitations. In this page , the choice of architecture and other trade offs are detailed.

The requirement of settling error and settling time translates to the required gain and bandwidth of the opamps. Error budgeting to stating and dynamic error again is decided on the basis of gain and bandwidth of the opamps and the settling budget given to linear settling and slewing is decided by the basis of distortion and slewing tolerable. The calculations for these are given in page 4 and 5.

After looking at the required gain of ~100dB and open-loop UGB of ~1.6GHz[1] of the opamp first we tried to explore the possible architecture that can be used. Using single stage and two stage opamps were first explored where we found that the use of two stage architecture although can be used to give a high gain but this would require compensation to a stable operation which in turn will result in formation of doublets at low frequencies lowering accuracy and increased settling time.

Moving on single stage architectures, we felt that it might be possible to gain high enough open loop UGB but a very high gain of ~100dB looks unrealistic without any special trick. The idea of gain boosting seems like a reasonable choice. Among the single stage architectures, we explored the most standard types namely Telescopic and Folded cascade. Folded cascade opamp would be more power hungry as it will either require double the current than its telescopic counterpart or would give higher slew rate limitations based on how much current we burn in the folding branch. At the same time, the stability due to the pole at the folding node could result in problems in stability on the other hand, the telescopic architecture will have just single pole[2] giving better stability. Among the noise and SNR issues, its well known that the folded cascade opamps are worse than telescopic opamps in terms of noise performance due to the noise contribution from the current source in the folding branch. Concluding, telescopic architecture looks more promising overall performance like power, stability and noise issues and so we decided to built the telescopic opamp with gain boosting.

To get the higher output swing, it was decided to have Δ=0.15 for all the transistors of the telescopic opamp. The design of the gain boosting opamp was done keeping in mind the position of its UGB in relation to that of main telescopic opamp[3]. Later, the transistors sizing was done using the approach discusses in class.

At this point I would like to mention that, with the approach discussed in class, I designed the three opamps in such a short time that I had never done before!

While the current sources and biasing transistors can be designed to minimize the power consumption without creating other disadvantages, the biasing circuits[4], common mode feedback circuits were design was centered towards simplicity, flexibility and available time to ‘market’.

[1] See the calculations for these values.
[2] Being fully differential
[3] Refer page 4,5 for detail.
[4] Please see the note on page three for high power consumption.

II. Schematics and Operating Point Analyses

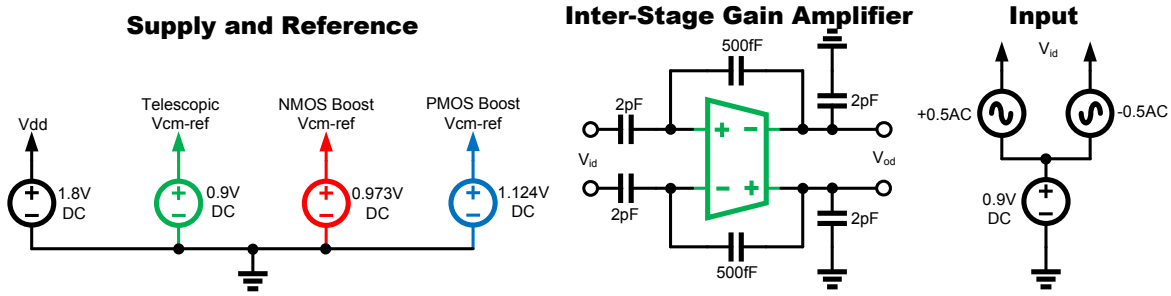

Figure 1) Fixed Supplies, Inter-Stage Gain Amplifier, Test Input Signals

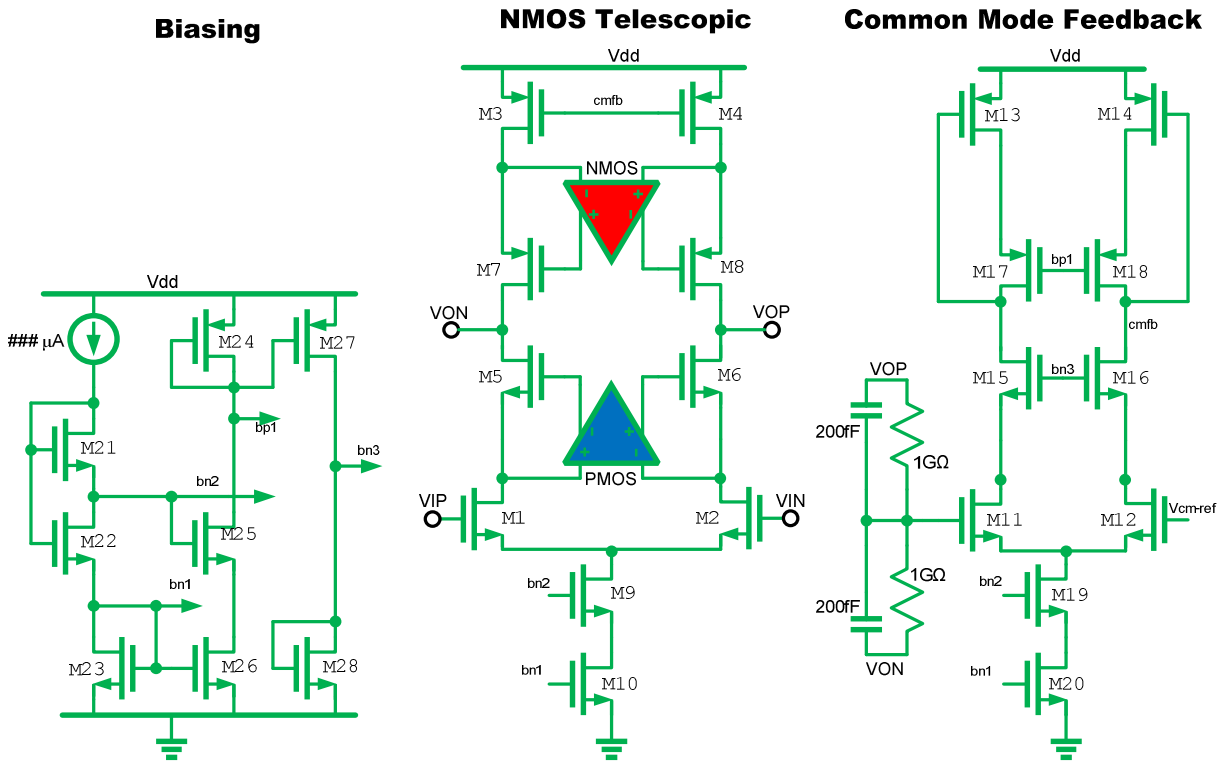

Figure 2) Fully Differential Telescopic Inner-Stage Gain Amplifier

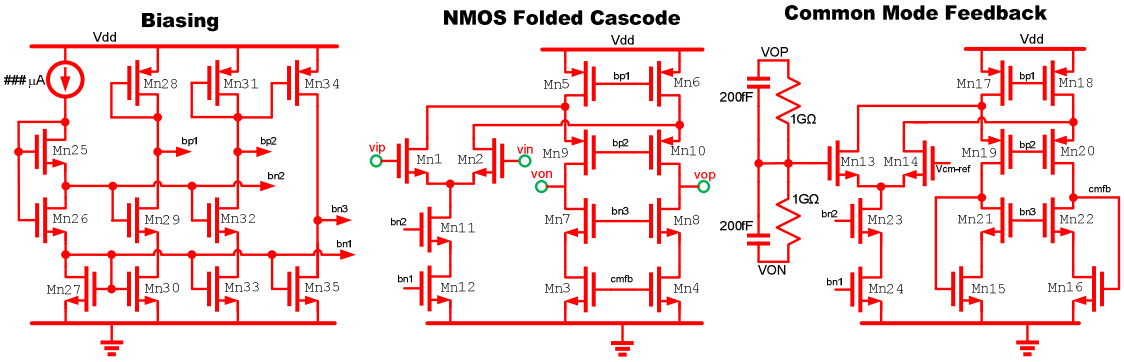

Figure 3) Fully Differential NMOS Input Folded Cascode Gain Boost Amplifier

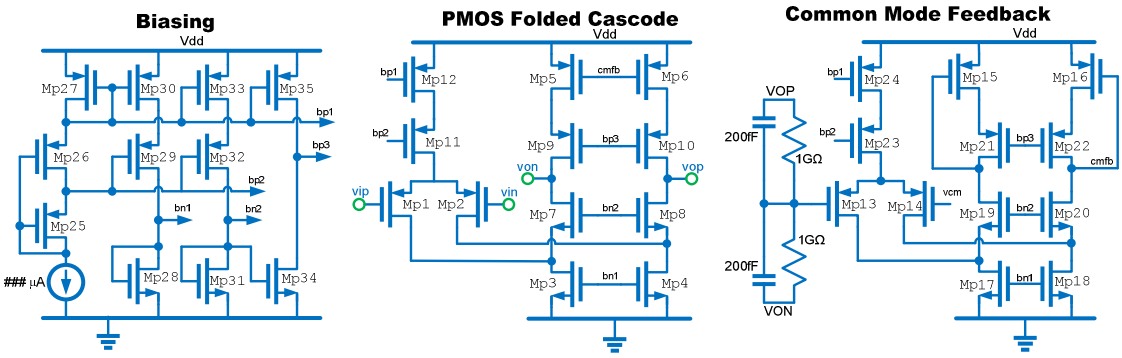

Figure 4) Fully Differential PMOS Input Folded Cascode Gain Boost Amplifier

Table 1) DC Operating Points

Telescopic							NMOS Gain Booster							PMOS Gain Booster						
MOS	Mult	W	L	I_D	g_m	Δ	MOS	Mult	W	L	I_D	g_m	Δ	MOS	Mult	W	L	I_D	g_m	Δ
		[µm]	[nm]	[µA]	[mS]	[mV]			[µm]	[nm]	[µA]	[mS]	[mV]			[µm]	[nm]	[µA]	[mS]	[mV]
M1	30	10	180	3041	53.5	85.1	Mn1	25	10	180	2016	34.59	89.96	Mp1	70	10	180	999	18.75	83.8
M2	30	10	180	3041	53.5	85.1	Mn2	25	10	180	2016	34.59	89.96	Mp2	70	10	180	999	18.75	83.8
M3	71	10	180	3041	40.2	126	Mn3	12	10	250	2323	20.74	156.4	Mp3	9	10	180	2020	19.22	140.0
M4	71	10	180	3041	40.2	126	Mn4	12	10	250	2323	20.74	156.4	Mp4	9	10	180	2020	19.22	140.0
M5	23	10	180	3041	42.2	118	Mn5	52	10	180	4339	40.69	169.1	Mp5	13	10	180	1021	9.61	166.0
M6	23	10	180	3041	42.2	118	Mn6	52	10	180	4339	40.69	169.1	Mp6	13	10	180	1021	9.61	166.0
M7	71	10	180	3041	41.5	123	Mn7	21	10	500	2323	21.58	170.6	Mp7	11	10	500	1021	10.41	157.3
M8	71	10	180	3041	41.5	123	Mn8	21	10	500	2323	21.58	170.6	Mp8	11	10	500	1021	10.41	157.3
M9	70	10	250	6082	82.3	114	Mn9	84	10	500	2323	21.28	177.6	Mp9	42	10	500	1021	9.96	168.2
M10	65	10	250	6082	74.6	118	Mn10	84	10	500	2323	21.28	177.6	Mp10	42	10	500	1021	9.96	168.2
M11	30	10	180	3014	45.2	102	Mn11	18	10	180	4033	45.15	128.1	Mp11	26	10	180	1998	21.32	159.2
M12	30	10	180	3043	45.5	102	Mn12	18	10	180	4033	39.08	139.1	Mp12	26	10	180	1998	17.21	169.2
M13	71	10	180	3014	40	125	Mn13	9	10	180	1877	22.5	117.6	Mp13	70	10	180	441.6	9.12	59.6
M14	71	10	180	3043	40.2	126	Mn14	9	10	180	2013	23.33	121.2	Mp14	70	10	180	997.6	18.36	76.1
M15	23	10	180	3014	41.3	105	Mn15	12	10	250	2430	20.74	160.1	Mp15	13	10	180	1435	9.07	204.9
M16	23	10	180	3043	43.6	105	Mn16	12	10	250	2315	20.61	156.3	Mp16	13	10	180	1022	9.62	166.1
M17	71	10	180	3014	41.3	125	Mn17	52	10	180	4307	40.14	169	Mp17	9	10	180	1877	16.95	139.9
M18	71	10	180	3043	41.6	126	Mn18	52	10	180	4328	40.51	169.1	Mp18	9	10	180	2019	19.20	140.0
M19	70	10	250	6058	79.2	115	Mn19	40	10	250	2430	23.28	173	Mp19	11	10	500	1435	12.18	182.0
M20	65	10	250	6058	74.1	118	Mn20	40	10	250	2315	22.73	169.3	Mp20	11	10	500	1022	10.41	157.3
M21	63	10	250	6000	74.6	132	Mn21	12	10	250	2430	23.76	154.5	Mp21	42	10	500	1435	11.74	195.1
M22	1	140	250	6000	37	759	Mn22	12	10	250	2315	23.24	151.5	Mp22	42	10	500	1022	9.97	168.0
M23	63	10	250	6000	74.6	132	Mn23	18	10	250	3890	38.44	139.2	Mp23	26	10	180	1439	6.87	212.9
M24	18	10	180	6047	27.1	850	Mn24	18	10	180	3890	36.75	139.1	Mp24	26	10	180	1439	10.45	168.5
M25	70	10	250	6047	87.6	106	Mn25	4	9	180	4053	15.13	878.7	Mp25	1	65	180	2000	21.35	526.0
M26	63	10	250	6047	75.6	118	Mn26	1	45	180	4053	17.87	825.6	Mp26	26	10	180	2000	9.52	832.0
M27	18	10	180	5891	676	306	Mn27	4	9	180	4053	15.13	878.7	Mp27	26	10	180	2000	17.24	144.0
M28	1	35	250	5891	13.5	383	Mn28	10	10	180	4053	16.05	337.1	Mp28	1	23	180	2031	9.13	226.9
							Mn29	18	10	180	4000	44.4	127.6	Mp29	26	10	180	2031	21.66	157.4
							Mn30	18	10	180	4053	15.13	139.1	Mp30	26	10	180	2031	17.73	169.3
							Mn31	10	10	180	4038	16.02	174.8	Mp31	7	10	180	2045	19.78	142.1
							Mn32	18	10	180	4038	45.27	125.1	Mp32	26	10	180	2045	21.77	156.7
							Mn33	18	10	180	4038	39.17	139.2	Mp33	26	10	180	2045	17.97	142.1
							Mn34	40	10	180	4068	38.08	337.5	Mp34	6	10	180	1907	17.88	143.2
							Mn35	18	10	180	4068	39.65	249.7	Mp35	1	55	180	1907	8.38	313.0

Please Note: Single page was not enough to put all the schematic and table so an extra page was used. Sorry for inconvenience caused.

III. Simulated Performance Summary

Table 2) Simulated Performance Summary

Design parameter/variable	Simulated performance	Specification	Units
Supply voltage	1.8	≤ 1.8	[V]
Closed loop gain	4	4	[V/V]
Settling error (static + dynamic)	2.5×10^{-4}	≤ 2.5×10^{-4}	[%]
Load capacitance (C_L)	2	2	[pF]
Settling time	+/- 4.8	≤ 5	[ns]
Peak SNR	68.5	≥ 66	[dB]
Differential r.m.s. noise voltage	156.5	---	[μV]
THD (Fin = 1MHz)	-117.43	≤ -70	[dB]
THD (Fin = 49MHz)	-106.68	≤ -70	[dB]
Amplifier core power consumption	21.6[5]	Minimum	[mW]
Bias power consumption	64.8	Minimum	[mW]
Total power consumption	86.4	Minimum	[mW]
Differential DC loop gain (v_{od} =0)	107.8*β[6] = 92.99	---	[dB]
Differential DC loop gain (v_{od} = $v_{od,max}$)	107.8*β = 92.99	---	[dB]
Differential loop-gain unity gain bandwidth	1153.6	---	[MHz]
Differential loop-gain phase margin	57.6	---	[deg]
Differential loop-gain gain margin	-19.98	---	[dB]
Common-mode loop-gain unity gain bandwidth	48.76	---	[MHz]
Common-mode loop-gain phase margin	80.94	---	[deg]

[5] 1) The bias branches carry the same power which can be reduced but changing the mirror ratio.
2) Also the gain boosting opamps were designed for high capacitive load (9pF) and thus consuming high current for the same bandwidth. Later it turned out that the loading on these gain boosting opamps were really small and to these opamps was loaded with extra capacitors as shown in the schematic. If gain boosters were designed to load close to actual load (3p) then the current requirement on these would be lot less to get the same bandwidth. These are the two main reasons for the high current consumptions. I really feel this power consumption is ridiculous and can surely be improved

[6] β is feedback factor found out to be 1/5.5 using simulation results and $\beta = \frac{f_{UGB,LG}}{f_{UGB,OLG}} = \frac{208MHz}{1.156GHz}$

V. Calculations

The calculations that follow are the order in which this operational transconductance amplifier (OTA) was designed. This process was not followed strictly in the initial design of the amplifier. However, the process represented in this section is the final calculation process which was followed for the resulting amplifier.

The amplifier design is divided into sections, starting with the determination of system level design constraints, and then moving into design of the main amplifier (telescopic) based upon this system level constraints. Transistor sizing is then undertaken for the top-level design using the g_m/I_D device sizing strategy used in ECE520 Handout 5 on Design-Oriented Transistor Sizing [1]. Then, an NMOS and a PMOS gain booster (folded cascode) are designed using the same g_m/I_D process to fit into the top level telescopic amplifier. The pole-zero doublets which can hamper transient response is designed so as to not degrade performance of the main telescopic amplifier [2].

a.) System Level Design Considerations [1]

Total Settling Error (ε_T) = {(static error (ε_S) + dynamic error (ε_D)} ≤ 2.5×10^{-4}

→ choose $\varepsilon_D = 2.3 \times 10^{-4}$ → Larger ε_D chosen because of gain dependence and availability of gain boosting. Lower bandwidth requirements (f_{UGB}) needed for (ε_S).

Static Error = $\varepsilon_T - \varepsilon_D = 2.5 \times 10^{-4} - 2.3 \times 10^{-4} = \varepsilon_S = 0.2 \times 10^{-4}$

a.1) System Level Dynamic Error Considerations [1], [3]

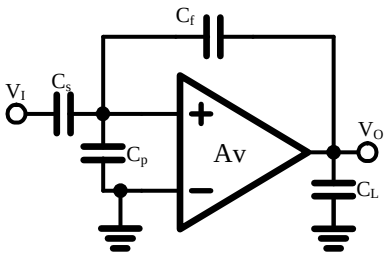

Figure 5) Circuit for Error Consideration

$$\frac{V_O}{V_I} = -\beta \frac{1-s\frac{C_f}{C_S}}{1+s\frac{C_L+(1-\beta)C_F}{\beta A_V}} \ , \ z = +\frac{A_V}{C_f} \ , \ p = -\frac{\beta A_V}{C_L+(1-\beta)C_f}$$

$$V_{O,Step} = -V_{I,Step}\ \frac{C_S}{C_F}\left[1-\left(1-{}^{p}/_{z}\right)e^{-t/\tau}\right]$$

$$with \quad \tau = \frac{C_{L,eff}}{\beta A_V} \ , \qquad C_{L,eff} = C_L + (1-\beta)C_f$$

For the case: $-{}^{P}/_{Z} \ll 1$: $\quad V_{O,Step}(t) = -V_{I,Step}\ \frac{C_S}{C_F}\left[1-e^{-t/\tau}\right] \quad and \quad \frac{t_S}{\tau} = -\ln(\varepsilon_D)$

t_s settles linearly; slewing non-linear ∴ larger t_s to minimize distortion → t_s = 4.75ns out of 5ns settling time

$$\tau = \frac{-t_s}{\ln(\varepsilon_D)} = \frac{1}{2\pi f_{UGB,LG}} = \frac{-4.75 \times 10^{-9}}{\ln(2.3 \times 10^{-4})} \rightarrow f_{UGB,LG} = 280\ MHz$$

$$\beta = \frac{C_f}{C_f + C_s + C_p} = \frac{f_{UGB,LG}}{f_{UGB,OLG}} \ , \qquad \frac{0.5pF}{0.5pF + 2pF + 0.5pF^{7}} = \frac{1}{6}$$

$$\beta = \frac{280\ MHz}{f_{UGB,OLG}} = \frac{1}{6} \rightarrow f_{UGB,OLG} = 1.680GHz$$

[7] Assuming 0.5pF is parasitic input capacitor.

a.2) System Level Static Error Considerations [1], [3]

$$\frac{V_O}{V_I} = -\frac{C_S/C_f}{1+\frac{1}{\beta A_{VO}}} = -\frac{C_S}{C_f}\left(1-\frac{1}{\beta A_{V0}}\right) \quad , \quad \frac{V_O}{V_I} = -A_{VO}$$

$$\varepsilon_S = \frac{1}{\beta A_{VO}} \rightarrow \frac{1}{\beta \varepsilon_S} = \frac{6}{0.2\times 10^{-4}} = A_{VO} = 300{,}000 = 109.54\ dB$$

b.) Design of Gain boosting opamps.

In this section we have described the specs that we decided for the gain boosting opamps. The chosen topology for the gain boosting opamps was fully differential folded cascode type. For the stability consideration the UGB of the gain boosting opamps should satisfy:

$$\beta\omega_{OL,UGB} < \omega_{GB,UGB} < \omega_{P2}$$

Where $\omega_{OL,UGB}$ is UGB of open loop amplifier, $\omega_{GB,UGB}$ is the UGB of the gain boosting opamps and ω_{P2} is the second pole of mail opamp. With constrain, the UGB of the gain boosting opamps was chosen to be around 400-500 MHz and the gain and phase margin was 50dB and 55 deg. respectively.

c.) $Peak\ SNR$[8] $= \frac{Maximum\ Signal\ Power}{Total\ Noise\ Power} = 10\log\left(\frac{\frac{(0.6)^2}{2}}{2.44*10^{-8}}\right) = 68.67dB$

d.) THD[9] $= \frac{\sum_{i=2}^{6} ith\ Harmonic\ Power}{Fundamental\ Frequency\ Power} = -48.4 - 61.28 == -106.68\ @\ 49MHz$

THD[10] $= \frac{\sum_{i=2}^{6} ith\ Harmonic\ Power}{Fundamental\ Frequency\ Power} = -52.94 - 64.49 = -117.43dB\ @\ 1MHz$

[8] Refer to the noise plot for the noise power and output swing plot for the signal power.

[9] Refer to the FFT for the power of harmonics and since the circuit is differential, even harmonics are not present.

[10] Refer to the FFT for the power of harmonics and since the circuit is differential, even harmonics are not present.

V. Simulation Results

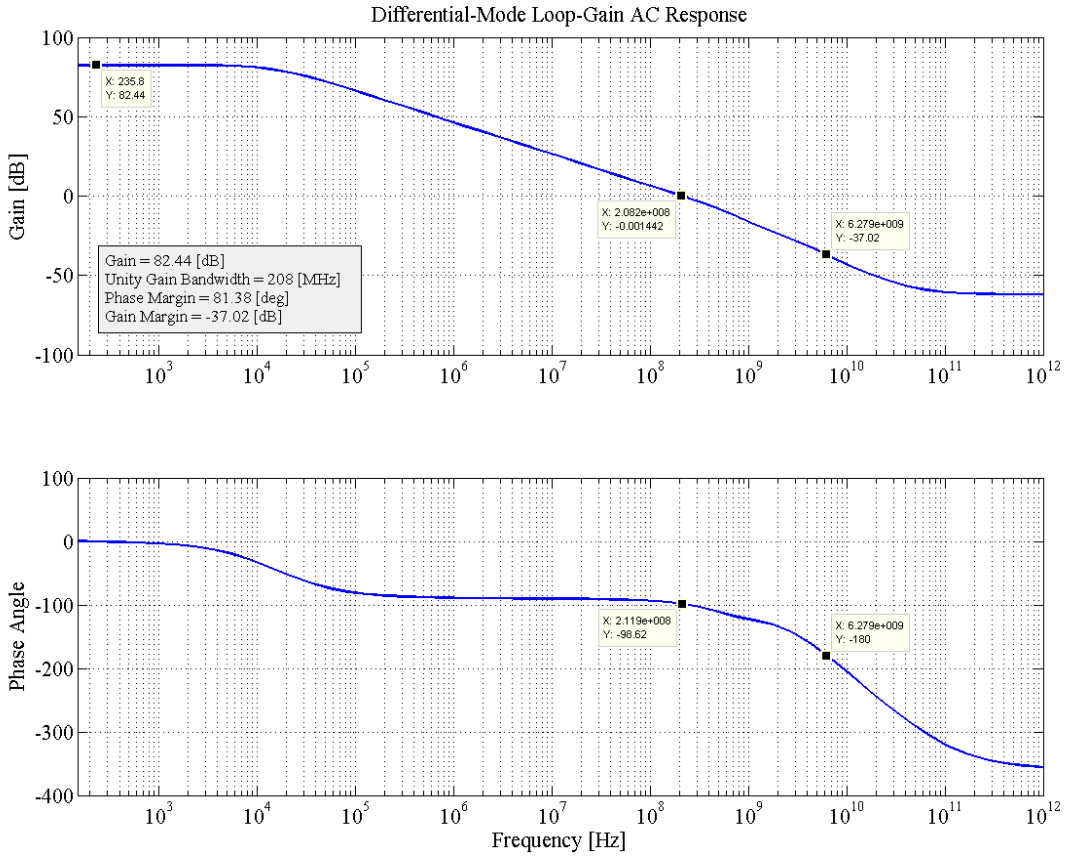

Figure 6) Differential-Mode Loop-Gain AC Response (Magnitude and Phase)

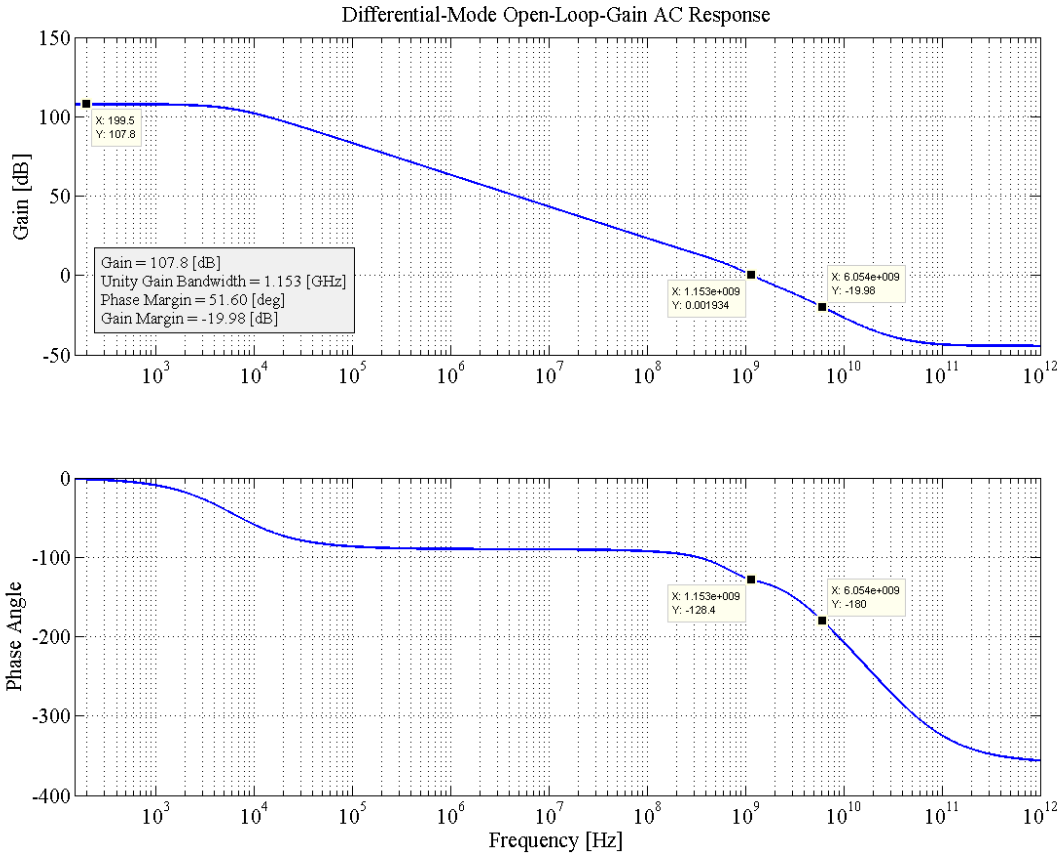

Figure 7) Differential-Mode Open-Loop-Gain AC Response (Magnitude and Phase)

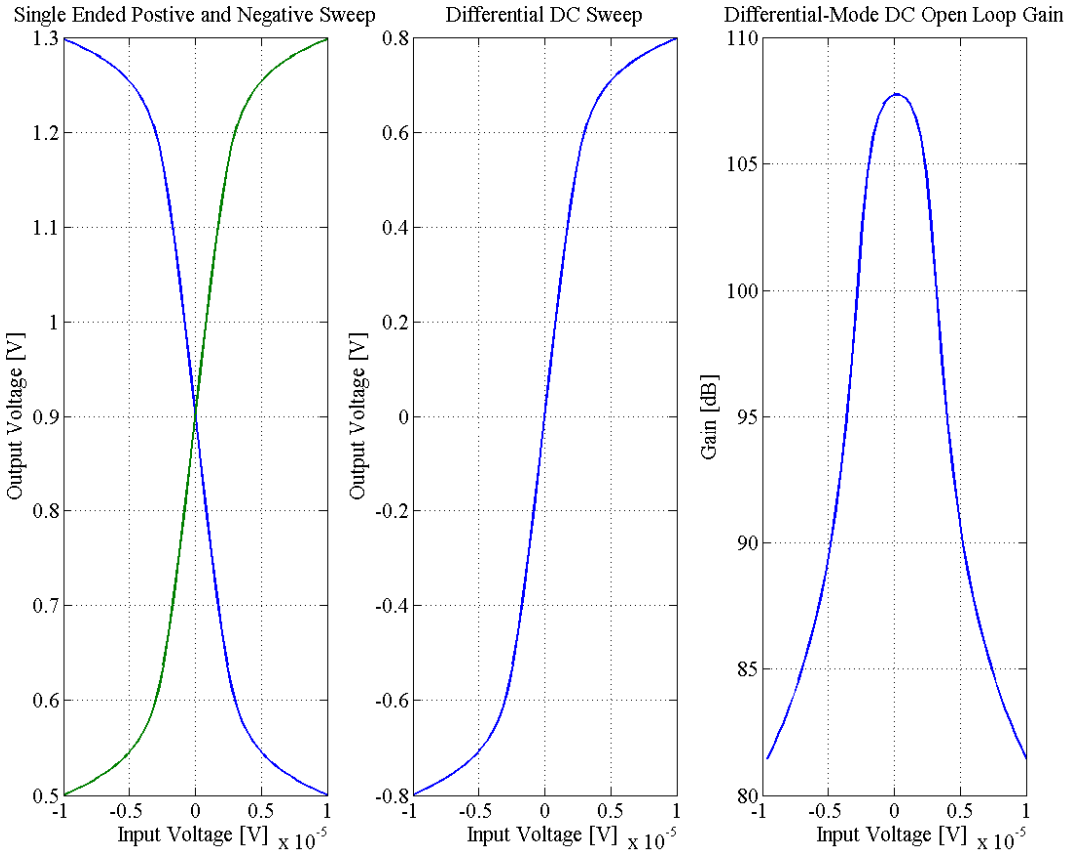

Figure 8) Differential-mode DC loop Gain vs. Differential Output Swing

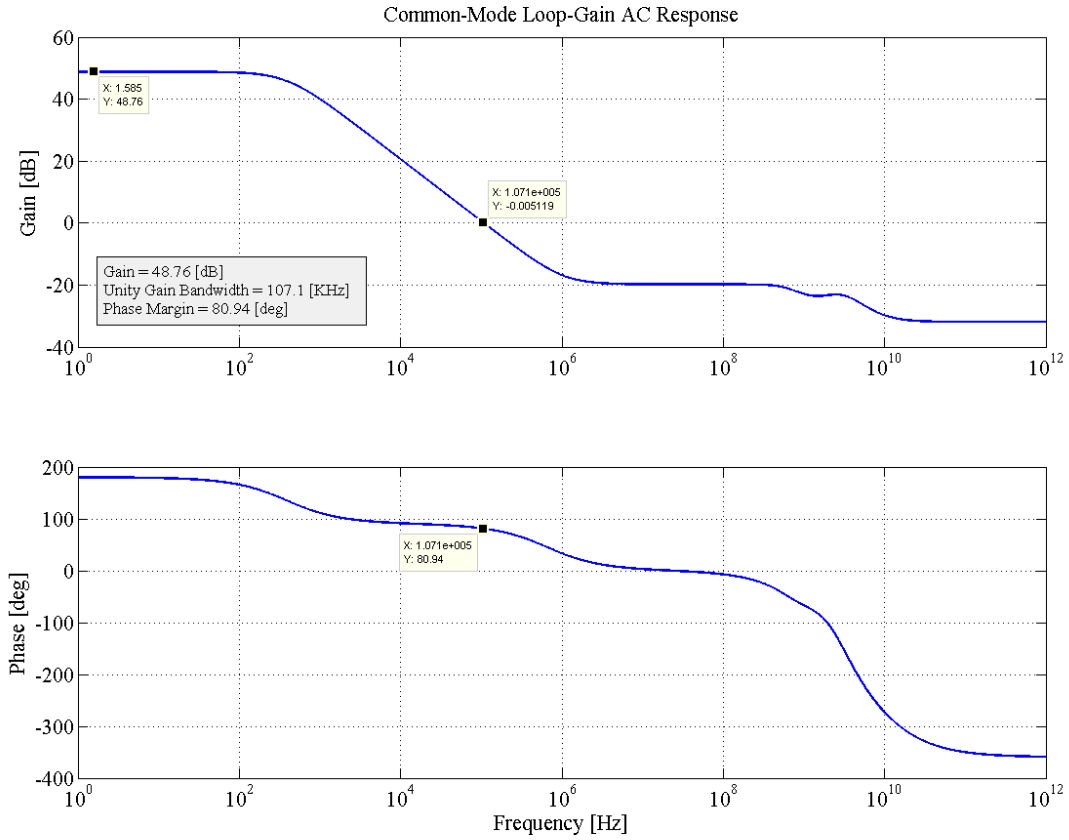

Figure 9) Common-Mode Feedback Loop-Gain AC Response

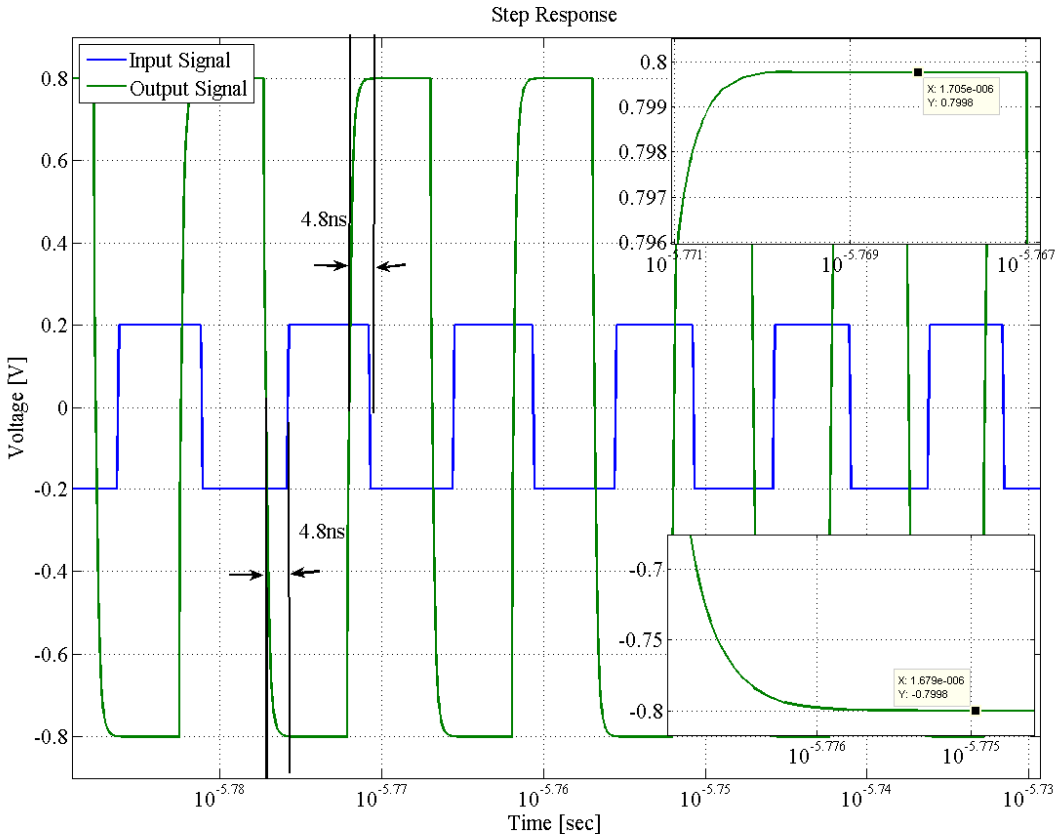

Figure 10) Positive and Negative Step Response with Settling Error and Settling Time

Positive settling time = 4.8 [ns]

Negative settling time = 4.8 [ns]

Positive settling accuracy = 799.8 [mV]

Negative settling accuracy = 799.8 [mV]

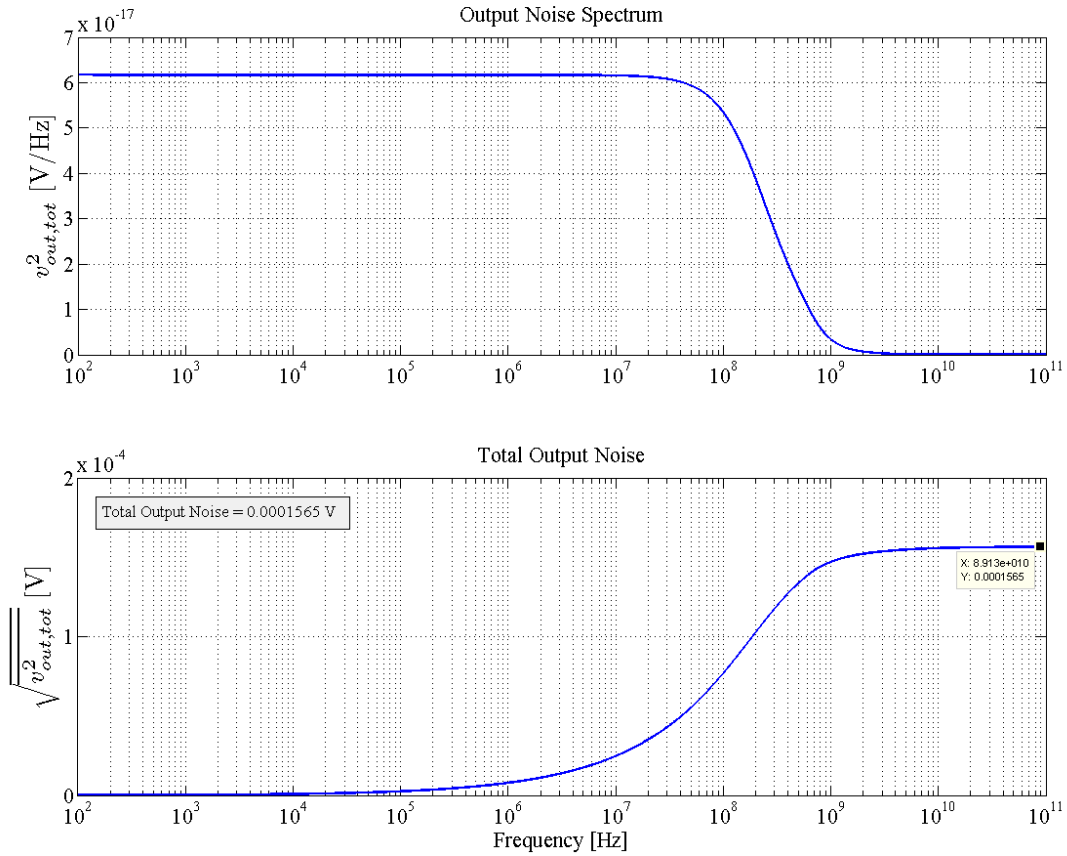

Figure 11) Output Noise Spectrum and Integrated Differential Output Noise

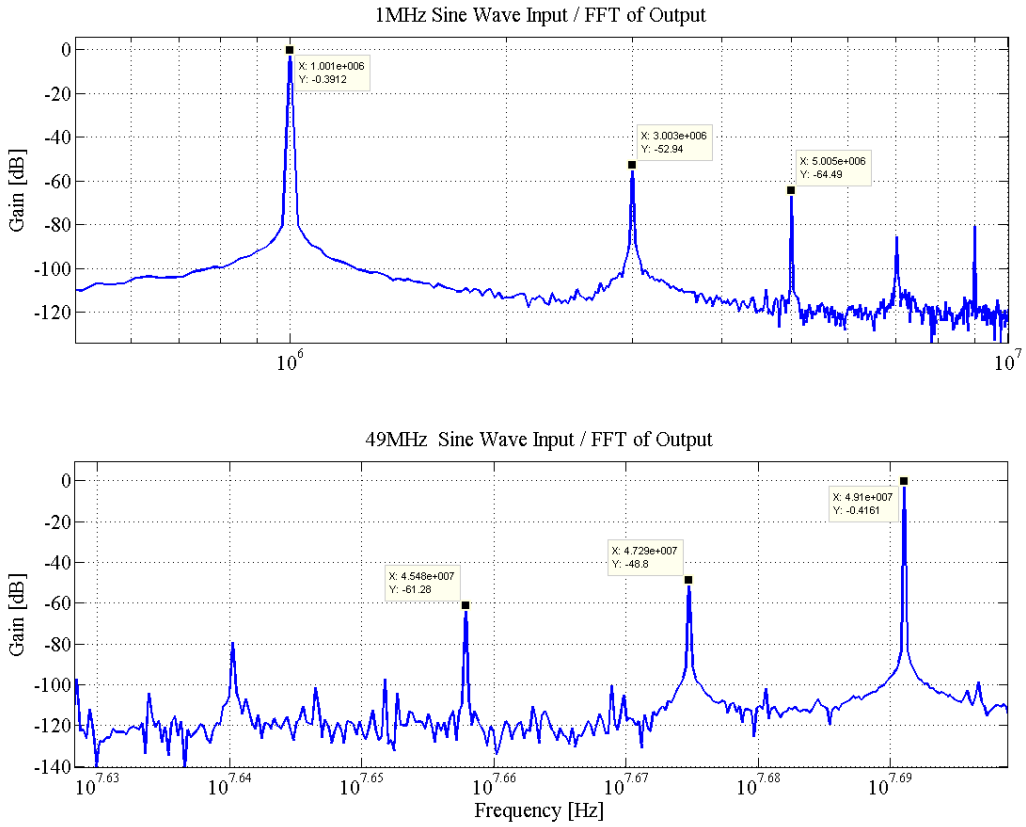

Figure 12) FFT of Output Spectrums of 1MHz and 49MHz Sine-Waves

VI. References

[1] Dr.Pavan Kumar Hanumolu, *ECE 520 Handouts 1 through 10.* Oregon State University: 2009.

[2] Dr.Nagendra Krishnapura, EE539:Analog IC Design lectures' and class notes, IIT Madras, 2008.

[3] ECE240, online lectures and slides, UC Berkeley,2006.

[4] Klaas Bult et.al. 'A fast settling CMOS op amp for SC circuits with 90-dB DC gain'

[5] Wang Jin et.al. 'Analysis and design of fully differential gain boosted telescopic cascode opamp'

[6] Flandre et.al. 'Improved Synthesis of Gain-Boosted Regulated-Cascode CMOS Stages Using Symbolic Analysis and gm/ID Methodology'

[7] Katsufumi Nakamura et.al 'An enhanced fully differential folded cascode opamp'

[8] Some of the last years reports from students how took this class before.

VII. Acknowledgement

We would like to thank Jacob, Hari Prasad, Manideep, Sachin, Amr, Tao, Chris, and Divya for all of the help and support which was rendered.